

WE CLAIM:

1. A dynamic logic circuit on a SOI substrate, comprising:

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a pull-down network comprising a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series
10 connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

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a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

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2. The dynamic logic circuit of claim 1 wherein said precharge circuit comprises a PMOS transistor.

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3. The dynamic logic circuit of claim 1 wherein said ground switch circuit comprises a NMOS transistor.

4. The dynamic logic circuit of claim 1 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

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5. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors;

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a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal
10 and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

15 6. The dynamic logic circuit of claim 5 wherein said precharge circuit comprises a PMOS transistor.

7. The dynamic logic circuit of claim 5 wherein said ground switch circuit comprises a NMOS transistor.

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8. The dynamic logic circuit of claim 5 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

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9. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network;
and

an output node which is connected to said first common node of said pull-down network.

10. The dynamic logic circuit of claim 9 wherein said precharge circuit comprises a PMOS transistor.

11. The dynamic logic circuit of claim 9 wherein said ground switch circuit comprises a NMOS transistor.

12. The static logic circuit of claim 9 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

13. A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel
connected PMOS transistors with a first and second common
5 node;

a precharge circuit connected to a clock signal and to
said first common node of said pull-down network;

10 a ground switch circuit connected to said clock signal
and to said second common node of said pull-down network;
and

an output node connected to said first common node of
15 said pull-down network.

14. The dynamic logic circuit of claim 13 wherein said
precharge circuit comprises a PMOS transistor.

20 15. The dynamic logic circuit of claim 13 wherein said
ground switch circuit comprises a NMOS transistor.

16. The static logic circuit of claim 13 wherein at least
one of said MOS transistors in said pull-down network has a
25 gate tied to a floating substrate body.